REMARKS

In response to the Office Action dated July 7, 2005, Applicant has amended the present application as indicated above. No new matter has been added by the current amendments. Applicant respectively requests for the entry of the amendments and reconsideration of the application in view of the amendments and the remarks set forth below.

Amendments to the Specification

The title of the invention has been amended to clearly indicate the invention to which the claims are directed.

Amendments to the Claims

Claim 7 has been cancelled without prejudice. Claim 1 has been amended. Upon entry of the amendments, Claims 1-4, 6 and 10 are pending in the application. Claim 1 has been amended to clearly define the limitations of "the upper address" and "the upper address bit." Thus, no new matter has been added by the current amendments. Therefore, Applicant respectfully requests for the entry of the amendments.

Claim Rejections under 35 U.S.C.§112

Claims 1-4, 6-7 and 10 are rejected under 35 U.S.C. 112, second paragraph.

The Examiner states that Claim 1 recites an upper address bit. However, further in the body of the claim, the Examiner states that the upper address is referred to and not specifically recited as the upper address bit of the register block. Applicant has amended "the upper address" to "the upper address bit" in order to overcome the rejections.

Also, the Examiner states that in Claim 7, the signals being input are unclear in nature and the repetition of some type of compensation to either the memory card module or the signals themselves is equally unclear and indistinct. In order to overcome the rejections, Applicant has canceled Claim 7 without prejudice.

Accordingly, Applicant respectfully requests the rejections to be withdrawn.

Claim Rejections Under 35 U.S.C.§103(a)

Claims 1-4, 6-7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horan et al (U.S. Patent No. 5,999,743).

The Examiner states that a memory card module including a PCI-to-memory controller of the invention corresponds to a system memory using 4-kilobyte pages of Horan.

In addition, the Examiner states that the functionality of the PCI-to-memory controller of the invention corresponds to that of the PCI/IDE controller, PCI/EISA/ISA bridge, PCI/SCSI bus adapter type of devices of Horan.

However, Horan does not teach or even suggest the memory card module including the PCI-to-memory controller of the invention. As shown in Figure 2 of Horan, the system memory 106 is connected to a core logic 204 through a memory bus 105 and the PCI/IDE controller 118, PCI/EISA/ISA bridge 116 and PCI/SCSI bus adapter 114 are connected to the core logic 204 through a PCI bus 109. That is, the system memory 106 is separated from the PCI/IDE controller 118, PCI/EISA/ISA bridge 116 and PCI/SCSI bus adapter 114. On the other hand, the PCI-to-memory controller of the invention is included in the memory card module. Therefore, the memory card module including the PCI-to-memory controller of the invention is structurally distinguishable from the system memory 106 of Horan.

Besides, the function of the PCI-to-memory controller of the invention differs from that of the PCI/IDE controller, PCI/EISA/ISA bridge or PCI/SCSI bus adapter. As recited in Claim 1 of the invention, the PCI-to-memory controller, which is disposed between an internal bus (corresponding to the PCI bus) and the memory module, controls access to a plurality of sub-memories. However, in Horan, the functions of the PCI/IDE controller 118, the PCI/EISA/ISA bridge 116 and the PCI/SCSI bus adapter 114 are to connect a SCSI bus 111, a EISA/ISA 113 bus and integrated drive electronics (IDE) to the PCI bus 109, respectively, as shown in Figure 2 and described in Col. 11, lines 1 to 12 of Horan. Therefore, the functions of the PCI-to-memory controller of the invention are distinguishable from those of PCI/IDE controller 118, PCI/EISA/ISA bridge 116 or PCI/SCSI bus adapter 114.

Furthermore, the Examiner states that a register block included in a PCI interfacing unit of the invention corresponds to a base address register of Horan. As described in Col. 12, line 65 to Col. 13, line 10, the base address register of Horan, which resides in Host-to-PCI bridge, is used by the system BIOS memory mapping software to allocate AGP device address space. The base address register is used to determine the size of AGP device address space to allocate the AGP device address space to the system memory. After the addresses required for the AGP controller are written to the base address register, BIOS determines the size of the required AGP device address space by scanning the returned value from the least-significant bit of the base address register upwards (toward the most-significant bit) in Horan. However, the register block of the invention is not used to determine the size of the AGP device address space. As recited in Claim 1 of the invention, the register block has a lower

address bit, an upper address bit and a select bit, wherein the lower address bit represents addresses included in the range of an address region within a memory map, the upper address bit represents an address set to be used when a memory address region is beyond the address region of the memory map, and the select bit is used to directly access the memory module. That is, the register block of the invention is used to control access to the memory according to the memory map and selects the memory module. Therefore, the use of the register block in accordance with the present invention is different from that of the base address register of Horan. Accordingly, Claim 1 is patentable over the Horan patent.

Conclusion

In view of the foregoing remarks, applicant respectfully submits that the present application is believed to be in condition for allowance. A favorable disposition to that effect is respectfully requested. Should the Examiner have any questions or comments concerning this submission, or any aspect of the application, she is invited to call the undersigned at the phone number listed below.

Respectfully submitted,

Date: October 4, 2005

For Anthony M. Insogna Reg. No. 35,203
By Michael Fainberg Reg. No. 50,441
JONES DAY
222 East 41st Street
New York, New York 10017
(212) 326-3939